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multiprocessor race condition register read write simulation OR verification dep Search Advanced Search

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1. Parallel computing - Wikipedia, the free encyclopedia

   The third and final condition represents an output **dependency**: When two ... This is known as a **race condition**. The programmer must use a lock to provide mutual exclusion. .... EX = Execute, MEM = Memory access, WB = **Register write** back) .... A symmetric **multiprocessor** (SMP) is a computer system with multiple ...
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2. [PDF] Testing Closed-Source Binary Device Drivers with DDT

   File Format: PDF/Adobe Acrobat - Quick View
   by V Kuznetsov
   For the purpose of access **verification**, DDT treats the ... driver would **register** open, **read**, **write**, and close ..... Various **race conditions** with interrupts while playing audio. Intel Pro/1000 .... file about its **expected** behavior, DDT may find bugs **that** .... **dependencies** through the path leading to a bug. DDT ...
   infoscience.epfl.ch/record/147243/files/ddt.pdf

3. [PDF] Analyzing Multicore **Dumps** to Facilitate Concurrency Bug Reproduction

   File Format: PDF/Adobe Acrobat - Quick View
   by D Weeratunge - 2010 - Related articles
   Core **dumps** are **expected** to contain a complete snap- ... program is that the **write** to x at 7 and the **read** at 11 are not atomic; thus, there is a **race** between ..... a CSV); we have yet to see such **conditions** in the bug reports we have examined. .... Execution Replay of **Multiprocessor** Virtual Machines. In VEE, pages ...
   www.cs.purdue.edu/homes/suresh/papers/asplos10.pdf

4. raw - Secure source code hosting and collaborative development ...

   NBIO: NBIO may have partially completed - e.g., **read** of 4096 may return ... with -1 **Multiprocessor** Support for Event-Driven Programs (Zeldovich's masters work, ... map in private memory as **read-write** (multi-threaded, so multiple may be .... user provides hints about file system operation **dependencies** to let FS ...
   github.com/yang/notes/raw/.../Systems.page - Cached

5. Instruction-Set **Simulation** and Tracing

   Jun 8, 2004 ... There is also a **simulators** mailing list. To subscribe, **write** to <majordomo@xsim.com>. ..... registers and an eighth status **register** that includes **condition** codes, ... **Multiprocessor simulation** may cause higher miss rates in the .... parallel execution of IU and FPU and operand **dependency** stalls. ...
   www.xsim.com/bib/index1.d/Index.html - Cached - Similar

6. [PDF] Summarizing **Multiprocessor** Program Execution with Versatile ...

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by K Asanovi• - 2006 - Cited by 6 - Related articles
Whenever any processor issues a **read** or **write** request prior to a sample point, ... **race conditions**. We use 100000-instruction measurement samples, ...
groups.csail.mit.edu/cag/scale/papers/kbarr-phd.pdf

7. English Arabic Technical Computing Dictionary

... Function, Functional, Functional database, Functional **dependency**, Functionality, ... **Read**-eval-print loop, Readme, **Read**-only, **Read** only, Readout, **Read**-**write**, ... Real-time, Real time, Real-time structured analysis, R **Race condition**, ... Symmetric **multiprocessing**, Symmetric **multiprocessor**, Sync, Synchronize, ...
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8. Specification-driven functional **verification** with Verilog PLI ...

Jan 28, 2007 ... 5.2 Ruby expression that determines whether all **registers** ..... of a scalable **multiprocessor**" and was found to have a 10% performance penalty, ... VPI's inherent **dependence** on simulator-driven functional **verification** were ..... (2) it has synchronization issues such as **race conditions**-which further ...
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The advent of chip **multiprocessors** (CMPs) has moved parallel programming ..... system compares the **read** and **write** sets of all concurrent transactions. ..... certain **race conditions**; resolves the situation in which a transaction with TID ..... printed in a file when the execution finishes using the **dump** function. ...
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checker for state machines that supports compositional **verification** [5,6]. Our .... **write** to non-thread-local memory, though certain MCP API calls may also ... -heuristic switch is not given, MCP ignores calls to mcp **register** heuristic(), ... encounter the **race condition**, so xxx always takes the value 444. ...
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cally using non-deterministic automata. The inherent non- determinism implies that when implemented in .... memory accesses, which inevitably produces race conditions. ..... verification of multiprocessor systems," Computers and Com- ...
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2. [PDF] Evaluating Non-deterministic Multi-threaded Commercial Workloads

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Feb 2, 2002 ... Ruby to capture timing-dependent race conditions and .... acteristic in shared-memory multiprocessor simulation ...
www.cis.upenn.edu/~milom/papers/caecw02_workloads.pdf - Similar

3. [PDF] Output-Deterministic Replay for Multiprocessor Programs

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Replay data races without annotation. ▪ Found in many apps, benign or erroneous .... Includes all non-deterministic data: e.g., thread ... (Verification Condition,. Floyd '67). 2. Solve for the unknowns using a formula solver ...
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simulation. We obtain the ..... What are **Race**. **Conditions**?: Some Issues and Formalizations. ACM ...
www.cs.wisc.edu/multifacet/papers/isca03_flight_data_recorder.pdf

5. [PDF] Two Hardware-based Approaches for Deterministic **Multiprocessor** Replay

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processor deterministic replay in general and memory **race** recording in particular. ... episodes E and F in an execution, the no-conflict **condition** of Equation 1 must hold. .... **simulator** configuration matches the baseline shown in Ta- ..... Evaluating **non-deterministic** multi-threaded commercial workloads. ...
iacoma.cs.uiuc.edu/iacoma-papers/cacm_highlight09.pdf

6. [PDF] Fast Functional **Simulation** with Parallel Embra

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effects and **race conditions**, it does not compromise overall memory consistency. .... by **multiprocessor simulation**, allowing **simulation** with ..... Xen) and **non-deterministic** parallel cache **simulation** (as in. Sparc-sulima). ...
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enumerate all **race conditions** with the current exec timek assignments. 8: for all permutations of events in superset R do. 9: call discrete event **simulation** ...
www.engr.colostate.edu/.../pubs/.../2009-MPDA_IEEE_TII-PasrichaGabe.pdf

8. [PDF] Soft Real-Time Fuzzy Task Scheduling for **Multiprocessor** Systems

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conditions happened. In heterogeneous systems which tasks have different time constraints algorithm have to avoid .... Speed and **Race**. After that, fuzzification is applied to the .... **Simulation** results show that by increasing the number of .... **non-deterministic** heterogeneous computing systems," in Proc. IEEE ...
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9. A Conservative Approximation Method for the **Verification** of ...

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of preemptive **multi-processor** systems is undecidable using **...** namics of events, **race conditions**, and the **non-deterministic** execution order of tasks. **...**
ieeexplore.ieee.org/iel5/4840551/4840552/04840586.pdf?arnumber...

10. Microprocessor **Verification** Blog

The goal of **multi-processor verification**, simply put, is to find errors that **... Non-deterministic** true-sharing is the most complex mode of sharing and **...**
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... Formal Verification of the Gigamax Cache Consistency ... - McMillan - Cited by 154

1. [PDF] Multiprocessor Memory Model Verification

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by P Loewenstein - 2006 - Cited by 2 - Related articles
verifying memory consistency. In SPAA'05: Proceedings of the 17th Annual ACM Symposium on ... Defines a "memory order" for each multiprocessor execution. ...
fm.csl.sri.com/AFM06/slides/Loewenstein-MemoryModel.pdf - Similar

2. [PDF] SPAA05 - MH05: Efficient Algorithms for Verifying Memory Consistency

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by C Manovit - Cited by 14 - Related articles
Memory consistency models, Multiprocessor verification,. Sequential Consistency, Total Store Order, Vector Clocks. 1. INTRODUCTION. The memory consistency ...
citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.112... - Similar

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by S Qadeer - 2003 - Cited by 32 - Related articles
K.L. McMillan and J. Schwalbe, "Formal Verification of the Encore Gigamax Cache Consistency Protocol," <i>Proc. Int'l Symp. Shared Memory Multiprocessors ...

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[17] S. Qadeer, "**Verifying** sequential **consistency** on shared- **memory multiprocessors** by model checking," IEEE Transac- tions on Parallel and Distributed ...
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5. [PDF] **Verifying** Sequential **Consistency** on Shared-**Memory Multiprocessors** ...

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8. Henzinger/Qadeer/Rajamani: **Verifying** Sequential **Consistency** for ...

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10. EETimes.com - Techniques for **verifying multiprocessor** designs

Multiprocessor, or MP, **verification** revolves around memory accesses. **...** interactions between caches of the various processors, eliminating **cache coherency ...**
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unusual case), then a non-atomic load can read a value ... cution of a test even in the face of race conditions such as the ones described above. ..... "Multiprocessor design verification for the PowerPC? 620 ...
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3. Race condition ordering and functional verification system and ...

Method and apparatus for creating a multiprocessor verification environment ..... the functional model sends a set of unique identifiers (e. g., ... In operation, the system for ordering race condition events according to the present ...
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on a variety of multiprocessor systems, including but not limited to a CMP ... We evaluate our race recorder with full-system simulation of a CMP system ..... example, the slicing plan is not unique. Bacon and Goldstein proposed a .... order) execution with minimum context switches, so that a race condition can be ...

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The caches are **non**- blocking and can be accessed with multiple outstanding misses. The sys- **....** Some of these activities are not **unique** to multi- processors. However, the increased traffic **...** allel programs have **race conditions**, which occurs when **.....** uation Using a **Multiprocessor Simulation**,"ACM Trans. Com- **...**
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6. **[PDF]** A Multithreaded Scheduler for a High-Speed Simulator

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implemented with multiple threads and runs on a **multiprocessor** system. **.....** advance the **simulation**, a run command is issued to the scheduler, which causes **.....** state of one **unique** bit in the vector. Thus, no **race condition** can occur. **...**
digitalcommons.unl.edu/cgi/viewcontent.cgi?article=1036&context...

7. TechOnline | Complete SoC Design, **Verification** Reign at DAC Exhibits

... non-compatible design-for-test (DFT) schemes, different reset techniques, and preferred **...** You can also detect problematic **race conditions** and combinatorial loops at the **...** The tool has a **unique** physical-modeling capability at RTL, **....** The new release of HUB includes a **multiprocessor simulation** capability to **...**
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8. **Non-unique** results in design **verification** by test programs **...**

by A Adir - 2003
[0009] **Verification** of **multiprocessor** designs present special **... non-unique** results in multiple resources under **conditions** of **non-unique** result propagation **...**
www.freepatentsonline.com/y2003/0130831.html

9. **[PDF]** Cache Coherence Protocols: Evaluation Using a **Multiprocessor ...**

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Using a **Multiprocessor Simulation** Model. JAMES ARCHIBALD and JEAN-LOUP BAER **....** This prevents a possible **race condition** if a cache does **.....** determined using a least recently used (LRU) stack (**unique** for each processor). **...**
citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.118.8940...

10. **[PDF]** An All-Software Thread-Level Data Dependence Speculation System **...**

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Jan 16, 2002 ... validation runs on a Sun Enterprise 4000 **multiprocessor**. .... to a shadow copy of each variable **unique** to each thread to provide ... We refer to this data layout strategy as **non**-merged. .... memory consistency models, such **race-conditions** are only ... Table 4: Machine parameters used in **simulation**. ...

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   Assura physical **verification** cannot address a **file** larger than 2 Gigabytes. **...** To run Assura DRC, LVS, or RCX in parallel on a **multiprocessor** system, place ? **...** A **dependency** graph consisting of rule queues is built from the **dependencies** in **....** The default memory allocation is based on internal **testing** of larger **...**
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4. **Testing** Device Drivers on Windows Platforms

   Live targets (local and remote) and **dump files** **...** with Hyberfile, with a **multiprocessor** device and multicore devices, **....** This **testing** includes metadata **verification** and a **dependency** check to verify that **...** USB Boot, and **Registry** Filter (RegFlt) are Embedded Enabling Features in Windows Embedded Standard 2009. **...**

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the Intel Pentium Pro's manipulation of control **registers**. [11]. Similarly, the Pentium 4 uses recovery to .... directory protocols can handle this **race**, but doing so adds ..... We use a repository of 2000 **files** (totalling ~50 MB). .... **Verifying** a. **Multiprocessor** Cache Controller Using Random **Test**. Generation. ...
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shared-memory **dependencies** to enable **multi-processor** ex- .... final core **dump**, we also obtain the final state of every mem- ..... initializes the **register state**, and starts the replay. ..... to the repository of 20000 **files** (totaling 480 MB). ... the highest overhead on offline analysis among all **test** appli- ...
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verification: it also justifies the choice of Lotos as a specification language .... Consequently, the complexity of the Rcc described in Vhdl **register** transfer level was ..... Therefore, a **test** consists in a collection of input **files**, ...
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theorem to this effect, for an x86-specific notion of **race**. The axiomatic style of definition is relatively easy to ..... to a code for the 32-bit **register** r32, followed by a 4-byte ..... served) data **dependency** from each instruction to the next, ... that is not exercised by **testing** or **verification** with respect ...
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test cases is presented for **multiprocessor verification** of. PowerPC 620m at the functional model level. .... used **registers**, and so on. The output of ItTPG is in a **file** ... tion variables that have defined **dependencies** (e.g. L2 ...

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